In the Claims:

1.-16. (Canceled)

17. (Currently Amended) A method of fabricating a capacitor of a semiconductor device, the method comprising:

forming a capacitor lower electrode on a semiconductor substrate;

forming a dielectric layer on the lower electrode; and

sequentially stacking a metallic layer and [[an]] a poly$Si_{1-x}Ge_x$ layer on the dielectric layer to form an upper electrode comprising the metallic layer and the poly$Si_{1-x}Ge_x$ layer.

18. (Original) The method of Claim 17 wherein the poly$Si_{1-x}Ge_x$ layer comprises a doped poly$Si_{1-x}Ge_x$ layer.

19. (Original) The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed by doping a poly$Si_{1-x}Ge_x$ layer with P or As.

20. (Original) The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed by doping a poly$Si_{1-x}Ge_x$ layer with B.

21. (Original) The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed by depositing a poly$Si_{1-x}Ge_x$ layer while simultaneously doping impurities.

22. (Original) The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is deposited and simultaneously activated.

23. (Currently Amended) The method of Claim 22, wherein the doped poly$Si_{1-x}Ge_x$ is deposited and simultaneously activated between about 350°C and about 550°C.

24. (Original) The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is deposited and then activation and thermal treatment is performed.

25. (Original) The method of Claim 24, wherein activation and thermal treatment is performed between about 400°C and about 550°C.

26. (Original) The method of Claim 17, wherein the metallic layer of the upper electrode comprises TiN, WN, TaN, Cu, W, Al, noble metals, oxide of the noble metals, and/or combinations thereof.

27. (Currently Amended) The method of Claim [[17]] 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed using low pressure chemical vapor deposition (LP CVD) using furnace type equipment, single wafer type equipment, and/or mini-batch equipment.

28. (Original) The method of Claim 17, wherein the lower electrode comprises a metallic layer.

29. (Original) A method of fabricating a capacitor of a semiconductor device, the method comprising:

forming a capacitor lower electrode on a semiconductor substrate;

forming a dielectric layer on the lower electrode; and

forming an $Si_{1-x}Ge_x$ layer on the dielectric layer at about 550°C or less.

30. (Original) A method according to Claim 29, further comprising:

thermally treating the $Si_{1-x}Ge_x$ layer at about 550°C or less.

31. (New) A method according to Claim 29 wherein the following is performed between forming a dielectric layer and forming an $Si_{1-x}Ge_x$ layer:

forming a metallic layer on the dielectric layer; and

wherein forming an $Si_{1-x}Ge_x$ layer comprises forming an $Si_{1-x}Ge_x$ layer on the metallic layer at about 550°C or less.

32. (New) A method according to Claim 29 wherein the $Si_{1-x}Ge_x$ layer comprises a poly$Si_{1-x}Ge_x$ layer.

33. (New) A method according to Claim 17 wherein the poly$Si_{1-x}Ge_x$ layer is formed at about 550° or less.

34. (New) A method according to Claim 29 wherein the lower electrode comprises a metallic layer.